FPGA Deployment and Integration for Medical 3D Image Reconstruction

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Introduction

Spinal disorders and bad posture are common and need to be monitored frequently. Currently, the diagnosis of the spine is evaluated through the use X-rays on the whole back, resulting in cumulative radiation exposure of internal soft tissue organs. Fast and accurate alternative systems exist, however their cost is high. The aim of this study is to develop a low-cost system able to reconstruct the surface of the back accurately and rapidly.

Materials and Methods

Structured light is an accurate technique to obtain a 3D reconstruction of an object [1]. However, it requires numerous projections, acquisitions, and thus a lot of data to process. The reconstruction algorithm has been implemented in the Hard-Processor-System (HPS), which communicates with a Field Programmable Gate Array (FPGA). A top-down approach was followed: it consists in the analysis of the algorithm from a high-level language, followed by the implementation on the HPS and finally the implementation of the digital logic modules for the FPGA.

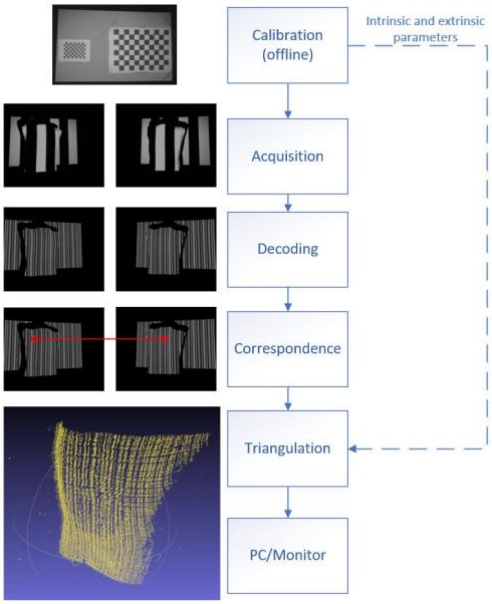

Fig. 1 : Acquisition and reconstruction chain: Two cameras at the same height capture the scene obtained by Gray code projections. The images are then processed to assign unique values to each pixel. Once the corresponding pixels are found, triangulation can be performed and the point cloud reconstructed.

Results

The current reconstruction of a single point cloud takes 10.27 seconds (CPU: Intel i7-7500 2.70 GHz). Therefore, a new embedded system was employed. The reconstruction was programmed in C++ to be cross-compiled and executed in the HPS, while the decoding logic modules were developed for the FPGA. Simulating the parallelism in the analysis phase, the background reconstruction can be avoided and save up to 80% of the point cloud vertices.

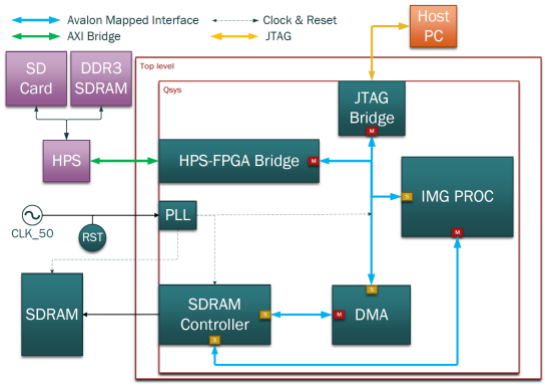

Fig. 2 : Proposed system: the SD card contains the acquisitions obtained through the cameras. The HPS reads the acquisitions and transmits them to the FPGA via a control program. The components of the FPGA process and save the data within the SDRAM connected to it. Values can be read back by HPS or computer via JTAG.

Discussion

This work suggests that by using parallelism techniques, the FPGA should accelerate the process. The FPGA programmed so far is not yet capable of real-time data processing, however, it has a basis of operation that can be improved. The tests performed demonstrated the feasibility of processing data in parallel, while the results confirmed the necessity. While the FPGA remains a valid solution for processing data rapidly, the use of a GPU should be critically evaluated, because of its capacity to process data in parallel. Faster memories with multiple accesses simultaneously increase parallelism. The division of tasks between FPGA and HPS should be optimized.

References